providing a dielectric protective layer over the contact bearing surface of said semiconductor chip, said dielectric protective layer having apertures for said chip contacts;

providing a compliant layer over said dielectric protective layer and over the central region of the contact bearing face of said semiconductor chip, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer; and

selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer, wherein each said bond ribbon electrically connects one of said chip contacts to an associated conductive terminal disposed on the top surface of said compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer and have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer.

36. (New) The method according to Claim 1, further comprising after selectively electroplating said bond ribbons, providing a second dielectric protective layer over exposed elements on the terminal side of said package, wherein said second dielectric protective layer has a plurality of apertures extending therethrough for providing access to said terminals.

37. (New) The method according to Claim 1, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting

polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

38. (New) The method according to Claim 1, further including the step of providing an encapsulant layer atop an exposed surface of said bond ribbons.

39. (New) The method according to Claim 4, wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

40. (New) The method according to Claim 4, further including the step of providing a second dielectric layer atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals.

41. (New) The method according to Claim 1, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip.

42. (New) The method according to Claim 1, further including before providing the compliant layer, plating a barrier metal atop the contacts of said semiconductor chip, wherein said barrier metal reduces voiding at an interface between the contacts and said bond ribbons.

43. (New) The method according to Claim 1, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further including dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

44. (New) The method according to Claim 1, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages, the method

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further including the step of dicing said adjacent packages after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

45. (New) A method of making a compliant microelectronic package comprising:

providing a microelectronic element having a first surface and a plurality of contacts disposed on the first surface thereof;

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providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more sloping edge surfaces extending between the top and bottom surfaces of said compliant layer, wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer; and

selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer for electrically connecting said contacts to conductive terminals overlying the top surface of said compliant layer, wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer.

46. (New) The method as claimed in claim 45, wherein the contacts are disposed in a first region of the first surface of said microelectronic element, and said compliant layer overlies a second region of the first surface of said microelectronic element, and wherein the sloping edges of said

compliant layer extend along one or more borders between the first and second regions of the first surface of said microelectronic element.

47. (New) The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

48. (New) The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes electrolessly plating a conductive material over the top of said package and selectively etching away portions of said conductive material.

49. (New) The method as claimed in claim 45, further comprising:

before the providing a compliant layer step, providing a first dielectric protective layer over the first surface of said microelectronic element, the first dielectric layer having a plurality of apertures in substantial alignment with said contacts for providing access to said contacts, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

50. (New) The method as claimed in claim 49, the selectively forming flexible bond ribbons step including electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

51. (New) The method as claimed in claim 45, further including the step of providing a dielectric cover layer over said compliant layer and said bond ribbons after the step of selectively forming said bond ribbons, wherein said dielectric cover layer has a plurality of apertures for accessing said terminals therethrough.

52. (New) The method as claimed in claim 45, further including the step of providing an encapsulant layer over an exposed surface of said bond ribbons.

53. (New) The method as claimed in claim 52, further including the step of providing a second dielectric protective layer atop the encapsulant layer, wherein the second dielectric protective layer has a plurality of apertures for accessing said terminals therethrough.

54. (New) The method as claimed in claim 45, further including before the step of forming said bond ribbons, depositing a barrier metal atop said contacts, wherein said barrier metal minimizes voiding between said contacts and said bond ribbons.

55. (New) The method as claimed in claim 45, wherein the method is applied to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further comprising separating said packages after the selectively forming elongated, flexible bonds ribbons step.

56. (New) The method as claimed in claim 45, wherein the method is applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding plurality of compliant semiconductor chip packages, the method further comprising separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating said bond ribbons.

57. (New) The method as claimed in claim 45, wherein the sloping edge surfaces of said compliant layer extend in both vertical and horizontal directions.